IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device with an ESD protective combination, comprising:

a first guard ring;

a first MOS transistor array formed in a region surrounded by said first guard ring and having a plurality of MOS transistors;

a second guard ring adjacent to said first guard ring; and

a second MOS transistor array formed in a region surrounded by said second guard ring and having a plurality of MOS transistors, wherein a channel length of each of said MOS transistors in said second MOS transistor array is larger ~~greater~~ than that of each of said MOS transistors in said first MOS transistor array.

2. (original) The semiconductor device according to claim 1, further comprising a first isolation portion formed between said first guard ring and said first MOS transistor array, and a second isolation portion formed between said second guard ring and said second MOS transistor array.

3. (original) The semiconductor device according to claim 1, wherein gates of said MOS transistors in said first MOS transistor array are electrically connected to each other, and gates of said MOS transistors in said second MOS transistor array are electrically connected to each other.

4. (original) The semiconductor device according to claim 1, wherein gates of said MOS transistors in said first MOS transistor array are grounded, and gates of said MOS transistors in said second MOS transistor array are grounded.